REMARKS

Claims 17-40 are all the claims pending in the application.

I. Objection to the Claims

Claims 18, 19, 23, 24, 28, 29, 33, 34 and 37-40 were objected to for the reasons set forth on page 4 of the Office Action. In particular, Applicants note that the Examiner has indicated that the above-noted claims do not further limit the subject matter of a previous claim.

While Applicants do not agree with the Examiner's position, in order to expedite prosecution, Applicants have amended claims 19, 24, 29, 34 and 37-40 such that these claims clearly further limit the subject matter of a previous claim, and have amended claims 18, 23, 28 and 33 such that these claims are now in independent form.

In view of the foregoing, Applicants kindly request that the above-noted objection be reconsidered and withdrawn.

II. Claim Rejections under 35 U.S.C. § 112, first paragraph

Claims 17-40 were rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement.

In particular, with respect to claim 17, the Examiner has taken the position that the "judging" step recited therein is not supported by the specification, and is therefore considered to be new matter. Applicants respectfully disagree.

Regarding the "judging" step of claim 17, Applicants initially note that this step has been amended so as to recite "judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main

data, which is one of a plurality of bytes of data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved."

Based on the Examiner's comments in the Office Action, it appears as though the Examiner is taking the position that the "judging" step of claim 17 is not supported by the specification because none of the individual steps shown in Fig. 5 of the present application (e.g., S105, S111, S113, S115 and S116) recite precisely what is set forth in the "judging" step of claim 17.

To the extent that the Examiner is taking this position, Applicants respectfully submit that there is no requirement that the language utilized in a particular step of claim 17 directly correspond to one of the individual steps shown in the flowchart of Fig. 5. Indeed, as is clearly set forth in MPEP 2163.03, "[t]he subject matter of the claim need not to be described literally (i.e., using the same terms or *in haec verba)* in order for the disclosure to satisfy the description requirement (emphasis added)".

In this regard, Applicants note that while none of the individual steps shown in the flowchart of Fig. 5 are specifically identified as "judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved", that the flowchart shown in Fig. 5, along with the corresponding description in the specification, provides support for such a feature, as will be described below.

In particular, regarding the description in the specification with respect to step S115 as shown in Fig. 5, Applicants note that the specification indicates that "[s]ince the main data

between sub data or the main data between sub data and SY have the same erasure position, erasure position information should be set at only the boundary between the main data area and the sub data area or the SY area" (emphasis added) (see page 16, lines 2-6 of the specification), and that "[w]hen the result of the judgement in step S115 is 'No', … the erasure position information at the same byte position in the previous code line is used…" (see page 16, lines 11-13) (see also Fig. 4(b) which shows the sync data area (SY), the sub data areas (SD) and the main data areas (MD)).

In other words, according to the above-noted disclosure on page 16 of the specification, erasure position information is set at only the boundary between, for example, the main data (MD) area and the sub data (SD) area, and because the main data between the sub data have the same erasure position, when it is judged that a byte position of a target code line is not at a boundary, the erasure position information at the same byte position in the previous code line is used. Thus, because the erasure position is only set for the main data at byte positions which are located at the above-described boundary between, for example, the MD area and the SD area, for all other byte positions of the main data of the target code line (i.e., the byte positions that are not at a boundary), the erasure position information at the same byte position of the previous code line is used.

Taking the above-noted disclosure into account, Applicants note that for byte positions of the target code line, the utilization of erasure position information at the same byte position of the previous code line inherently requires that there be a judgment as to whether a byte of the main data of the target code line is between the same two bytes of sub data as the previous code line. In other words, without performing such a judgment, it would not be possible to determine whether

the erasure position information at the same byte position of the previous code line should be utilized as the erasure position information at a certain byte position of the target code line.

Moreover, regarding the phrase "before being deinterleaved" in the above-noted "judging" step, Applicants note that the interleaved nature of the main data is evident from the byte positions shown in Fig. 4(c) of the present application.

In view of the foregoing, Applicants respectfully submit that the specification provides adequate support for the above-noted language recited in claim 17 of "judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved".

Accordingly, Applicants kindly request that the Examiner reconsider and withdraw the above-noted rejection of claim 17. In this regard, as noted above, the MPEP explains that the subject matter of a claim "need not to be described literally (i.e., using the same terms or *in haec verba)* in order for the disclosure to satisfy the description requirement" (see MPEP 2163.02).

With respect to claim 20, the Examiner has indicated that the feature recited therein drawn to the "judging" step is not supported by the specification. Initially, Applicants note that claim 20 has been amended so as to recite "judging that the first byte of main data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order."

Regarding support for the above-noted feature, Applicants note that the specification

provides support for this feature at least based on the description of Figs. 4(b) and 4(c), in conjunction with the disclosure at page 16 of the specification, where it is indicated that "[s]ince the main data between sub data or the main data between sub data and SY have the same erasure position, erasure position information should be set at only the boundary between the main data area and the sub data area or the SY area", and that "[w]hen the result of the judgement in step S115 is 'No', … the erasure position information at the same byte position in the previous code line is used…" (emphasis added) (see lines 2-14 on page 16 of the specification).

In other words, as described above, erasure position information is set at the boundary between, for example, the main data (MD) area and the sub data (SD) area, and because the main data between the sub data have the same erasure position, when it is judged that a byte position of a target code line is not at a boundary, the erasure position information at the same byte position in the previous code line is used.

Taking the foregoing into account, and turning to Figs. 4(b) and 4(c), Applicants note that based on the positional relationship between the code lines as shown in Fig. 4(c), and the arrangement of the SY areas, MD areas and SD areas as shown in Fig. 4(b), that if the "first byte of main data", which is located in the error correction target code line, is directly subsequent to a byte of sub data (in an SD area) or sync data (in an SY area) in a data recording order (see Fig. 4(b)), then the "second byte of main data", which is located in the "previous error correction code line", will not be located between the same two bytes of sub data as the first byte of main data.

As such, for byte positions of the target code line that are at the boundary, as described above, the erasure position information at the same byte position in a previous code line will not be used. Therefore, Applicants note that the setting of the erasure position information for a byte

of main data that is directly subsequent to a byte of sub data or sync data in a recording order will inherently include a judgment that the byte of main data of the target code line and the byte of main data of the previous code line do not exist between the same bytes of sub data.

In view of the foregoing, Applicants respectfully submit that the specification provides adequate support for the above-noted feature recited in claim 20 of "judging that the first byte of main data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order."

Accordingly, Applicants kindly request that the Examiner reconsider and withdraw the above-noted rejection of claim 20. In this regard, as noted above, the MPEP explains that the subject matter of a claim "need not to be described literally (i.e., using the same terms or *in haec verba)* in order for the disclosure to satisfy the description requirement" (see MPEP 2163.02).

Regarding claims 22, 25, 27, 30, 32 and 35, Applicants respectfully submit that the features recited in these claims are adequately supported in the specification for at least similar reasons as discussed above with respect to claims 17 and 20.

In view of the foregoing, Applicants respectfully submit that claims 17-40 comply with the written description requirement of 35 U.S.C. 112, first paragraph. Accordingly, Applicants kindly request that the above-noted rejection be reconsidered and withdrawn.

III. Claim Rejections under 35 U.S.C. § 112, second paragraph

Claims 17-40 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

Regarding claims 17, 18, 23, 27 and 33, the Examiner has indicated that the phrase "a plurality of pieces of sub-data" is indefinite. In particular, the Examiner has indicated that the

terms "piece" and "pieces" are not found in the specification.

Regarding the Examiner's position, Applicants point out that MPEP 2173.02 indicates that "a claim term that is not used or defined in the specification is not indefinite if the meaning of the claim term is discernible", and that the "test for definiteness under 35 U.S.C. 112, second paragraph, is whether 'those skilled in the art would understand what is being claimed when read in light of the specification'".

In this regard, while Applicants believe that the use of the terms "piece" and "pieces" would be understood by those of ordinary skill in the art, in order to expedite prosecution, Applicants have amended the claims by replacing the terms "piece" and "pieces" as used therein with the terms --byte-- and --bytes--, respectively. Applicants note that such terminology is used in the specification, and that one of ordinary skill in the art would readily understand the meaning and scope of such terminology.

In addition, regarding claims 17, 22, 27 and 32, Applicants note that the Examiner has also rejected these claims because the Examiner believes that the term "same" is a relative term that renders the claims indefinite. While Applicants do not agree with this position by the Examiner, in order to expedite prosecution, Applicants have removed the term "same" from claims 17, 22, 27 and 32.

In view of the foregoing, Applicants respectfully submit that claims 17-40 are in compliance with 35 U.S.C. 112, second paragraph. Accordingly, Applicants kindly request that the above-noted rejections be reconsidered and withdrawn.

IV. Claim Rejections under 35 U.S.C. § 102

Claims 17-20, 22-25, 27-30, 32-35 and 37-40 have been rejected under 35 U.S.C. §

102(e) as being anticipated by Marchant (U.S. 6,631,492).

Claim 17, as amended, recites the feature of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved. Applicants respectfully submit that Marchant does not disclose or suggest at least this feature of claim 17.

Regarding Marchant, Applicants note that Fig. 7 of this reference depicts a block of transverse ECC code word symbols 36' recorded on a band of longitudinal data tracks 24', with scratch detection fields 44a and 44b being recorded at each end of the block (see col. 6, lines 30-32). As disclosed in Marchant, scratch detection occurs when a positional coincidence is found between defective scratch detection symbols 48a and 48b in consecutive scratch detection fields, with the sections of data tracks connecting such defective scratch detection symbols 48a and 48b being flagged as suspect scratch locations (see col. 6, lines 40-44). In this regard, as explained in Marchant, all transverse ECC code word symbols 36' that are disposed on the flagged data track segments may then be processed by erasure correction (see col. 6, lines 40-44).

In the Office Action, with respect to the above-noted feature in claim 17 drawn to the judging of whether the first byte of main data and second byte of main data were located between the first and second bytes of sub data before being deinterleaved, the Examiner has taken the position that the scratch detection fields 48a, 48b of Fig. 7 of Marchant correspond to the bytes of main data, and has also taken the position on page 18 of the Office Action that "Marchant teaches an embodiment where scratch detection takes place before de-interleaving on read

Cross-interleaved ECC encoded data" (emphasis added). Thus, the Examiner is clearly taking the position that the data shown in Fig. 7 of Marchant is interleaved data. Applicants respectfully disagree.

In particular, Applicants point out to the Examiner that the disclosure in Marchant regarding cross interleaved codes is directed to Fig. 4 of Marchant (which is a "prior art" figure), but is not directed to Fig. 7. In this regard, Applicants note in Fig. 7 of Marchant, the defective scratch detection symbols 48a and 48b, as well as the ECC code word symbols 36', are not interleaved.

Therefore, regardless of which data in Fig. 7 of Marchant the Examiner is relying on as corresponding to the "first byte of main data" and the "second byte of main data", Applicants note that Fig. 7 includes no interleaving, and therefore, that the Examiner's reliance on Fig. 7 of Marchant for the teaching of "judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved" is incorrect.

In the event that the Examiner believes that it would have been obvious to modify Fig. 7 of Marchant such that the data shown therein is arranged in an interleaved manner, Applicants respectfully submit that if the data in Fig. 7 of Marchant was modified so as to be interleaved, that it would not be possible to determine the correct position where a scratch has occurred. In this regard, Applicants note that it is only because the data in Fig. 7 of Marchant is not interleaved, that it is possible to determine the correction position where a scratch has occurred.

In view of the foregoing, Applicants respectfully submit Marchant does not disclose, suggest or otherwise render obvious at least the above-noted feature recited in amended claim 17 of judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved. Claims 18-20 and 37 depend from claim 17 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 22, Applicants note that this claim recites the feature of judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 22 is patentable over the cited prior art, an indication of which is kindly requested. Claims 23-25 and 38 depend from claim 22 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 27, Applicants note that this claim recites the feature of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between

the first and second bytes of sub data before being deinterleaved.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 27 is patentable over the cited prior art, an indication of which is kindly requested. Claims 28-30 and 39 depend from claim 27 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 32, Applicants note that this claim recites the feature of a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 32 is patentable over the cited prior art, an indication of which is kindly requested. Claims 33-35 and 40 depend from claim 32 and are therefore considered patentable at least by virtue of their dependency.

V. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 21, 26, 31 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Marchant (U.S. 6,631,492) in view of Eachus (U.S. 3,685,016).

Claim 21 depends from claim 17; claim 26 depends from claim 22; claim 31 depends

from claim 27; and claim 36 depends from claim 32. Applicants respectfully submit that Eachus does not cure the above-noted deficiency of Marchant, with respect to claims 17, 22, 27 and 32. Accordingly, Applicants respectfully submit that claims 21, 26, 31 and 36 are patentable at least by virtue of their dependency.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Syuji MATSUDA et al.

By: /Kenneth W. Fields/ Digitally signed by /Kenneth W. Fields/ DN: cn=/Kenneth W. Fields/, o, ou, email=kfields@wenderoth.com, c=US Date: 2008.05.27 19:06:23 -04'00'

Kenneth W. Fields
Registration No. 52,430
Attorney for Applicants

KWF/krg
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
May 27, 2008